

Serial No. 10/026,532  
Docket No. PNDF-01197  
HIR.046

### REMARKS

Entry of this Amendment is proper because it narrows the issues on appeal and does not require further search by the Examiner.

The courtesy of Examiner Cynthia Britt in extending an interview to the undersigned attorney for Applicants is acknowledged with appreciation.

Claims 1-14 are presently pending in the application and have been amended to more particularly define the invention.

Claims 1-14 were rejected under 35 U.S.C. §112, second paragraph, with the contention that the claims are indefinite, and were rejected under 35 U.S.C. §102(e) as being anticipated by Whetsel, U.S. Patent No. 6,199,182. These rejections are respectfully traversed.

### **THE 35 USC §112, SECOND PARAGRAPH REJECTION**

Claims 1-14 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the Office Action contends that the terms “a first output terminal,” “a first input terminal,” “at least some of said plurality of flip-flops,” and “logic gate” are indefinite as used in the claims. This contention, and the rejection based on it, are traversed.

### **“A First Output Terminal” and “a First Input Terminal”**

The Office action contends that in order to comply with 35 U.S.C. §112, second paragraph, the claims which recite “a first output terminal” must also recite “a second output

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terminal,” and the claims which recite “a first input terminal” must also recite “a second input terminal.” This contention, and the rejection as based on it, are traversed.

Those claims which recited “a first output terminal” also recited “a scan output terminal.” Likewise, those claims which recited “a first input terminal” also recited “a scan input terminal.” Thus, the term “first” distinguished its output terminal or input terminal from the scan output terminal or scan input terminal. There is no requirement that when a “first” element is recited, additional such elements be designated “second.” The requirement is that the different claimed elements be distinguishable. The first output terminal thus was distinguished from the scan output terminal, and the first input terminal thus was distinguished from the scan input terminal.

Nevertheless, in the interest of expediting prosecution, the Examiner’s suggestion of changing “first” to “functional” has been adopted. Accordingly, the rejection on this basis is overcome.

**“At Least Some of Said Plurality of Flip-flops”**

The claims recited “a plurality of flip-flops” and “a like plurality of logic gates” and stated that each logic gate has an output terminal connected to an input terminal of a respective one of said plurality of flip-flops. As recognized in the Office Action, and as discussed during the interview, this wording indicates that there are the same number of logic gates as there are flip-flops, and that there is a one to one correspondence between the flip-flops and the logic gates.

The claims went on to recite that the scan path “serially connect(s) at least some of said plurality of flip-flops through the respective logic gates.” The Office action contends

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that this statement “seems to negate” the one to one correspondence. This contention, and the rejection as based on it, are traversed.

Figure 3, for example, depicts a plurality of flip-flops and a like plurality of logic gates, with each logic gate having an output terminal connected to an input terminal of a respective one of said plurality of flip-flops. Figure 3 also depicts a scan path serially connecting the plurality of flip-flops through the respective logic gates. An additional column of flip-flops, with respective logic gates, could be provided to the right of column n, but not included in the scan path. That would come within the disputed wording and yet, there would still be a one to one correspondence between the flip-flops and the logic gates. Thus, the one to one association was not negated by the wording.

Nevertheless, in the interest of expediting prosecution, “at least some of” has been deleted from the claims, thereby clearly overcoming the rejection, while recognizing that, since the claims recite the elements comprising the test circuit, the test circuit also might include additional elements.

#### Logic Gates

The first Office Action in this application rejected the claims under 35 U.S.C. §112, second paragraph, with the contentions, *inter alia*, that it is unclear from the claims and the specification what the function of the plural logic gates is, and that the logic gates could be another flip-flop, or any type of functional logic block. The current Office Action again rejects the claims under 35 U.S.C. §112, second paragraph, this time stating simply that the logic gates are claimed vaguely and not as required by the second paragraph of 35 U.S.C. §112. These contentions, and the rejection based on them, are traversed.

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“Logic gate” is not a vague or indefinite term; it is a term of art. Attached is a copy of the definition of “logic gate” from the Microsoft Press Computer Dictionary, Third Edition (1997). That definition simply says: “*See gate (definition 1).*” Also attached is a copy of the definition of “gate” from that same dictionary. Definition 1 is: “An electronic switch that is the elementary component of a digital circuit. It produces an electrical output signal that represents a binary 1 or 0 and is related to the states of one or more input signals by an operation of Boolean logic, such as AND, OR, or NOT. *Also called logic gate. See also gate array.*”

The claimed logic gates meet this definition. That is, the claimed logic gates are electrical switches that are elementary components of a digital circuit and that produce an electrical output signal that represents a binary 1 or 0 and is related to the state of its input signal.

It is accordingly submitted that the rejection based on “logic gates” should be withdrawn.

#### **Conclusion as to the 35 U.S.C. §112 Rejections**

During the interview, Examiner Britt indicated that the above amendments overcome the rejections based on 35 U.S.C. §112, second paragraph.

#### **THE 35 U.S.C. §102(e) REJECTION**

During the interview, Examiner Britt also indicated that the above amendments result in the claims distinguishing over Whetsel.

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### CONCLUSION

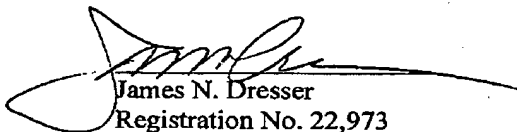
In view of the foregoing, Applicant submits that claims 1-14, all the claims presently pending in the application, are patentably distinct over the prior art of record and are allowable, and that the application is in condition for allowance. Such action would be appreciated.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned attorney at the local telephone number listed below to discuss any other changes deemed necessary for allowance in a telephonic or personal interview.

To the extent necessary, Applicant petitions for an extension of time under 37 CFR §1.136. The Commissioner is authorized to charge any deficiency in fees, including extension of time fees, or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: August 18 2005

  
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**CERTIFICATE OF FACSIMILE TRANSMISSION**

I hereby certify that I am filing this Amendment Under 37 C.F.R. §1.116 by facsimile with the United States Patent and Trademark Office to Examiner Cynthia H. Britt, Group Art Unit 2133 at fax number 571-273-8300 this 18th day of August, 2005.

  
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Best Available Copy

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**Computer  
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Third Edition

**Microsoft** Press

# Best Available Copy

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logical link control

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distinct from its physical realization in memory or storage. For example, a logical file might consist of a contiguous series of records, whereas the file might be physically stored in small pieces scattered over the surface of a disk or even on several disks. A logical file might also consist of some subset of columns (fields) and rows (records) extracted from a database. In this case, the logical file (or view) is only that information required by a particular application program or user.

**logical link control** \loj'ik lēnk' kən-trōl\ *n.* See IEEE 802 standards.

**logical operator** \loj'ik op'ər-ā'tər\ *n.* An operator that manipulates binary values at the bit level. In some programming languages, logical operators are identical to Boolean operators, which manipulate true and false values. See also Boolean operator, mask.

**logical record** \loj'ik rek'ərd\ *n.* Any unit of information that can be handled by an application program. A logical record can be a collection of distinct fields or columns from a database file or a single line in a text file. See also logical file.

**logical schema** \loj'ik skē'mā\ *n.* See conceptual schema.

**logic analyzer** \loj'ik an'ə-lī-zər\ *n.* A hardware device that facilitates sophisticated low-level debugging of programs. Typical features include the ability to monitor bus signals during execution, to halt execution when a given memory location is read or written to, and to trace back through some number of instructions when execution is halted for any reason. See also debugger.

**logic array** \loj'ik ə-ā'\ *n.* See gate array.

**logic board** \loj'ik bōrd\ *n.* Another name for motherboard or processor board. The term was used in conjunction with older computers to distinguish the video board (*analog board*) from the motherboard. See also motherboard.

**logic bomb** \loj'ik bom'\ *n.* A logic error in a program that manifests itself only under certain conditions, usually when least expected or desired. The term *bomb* implies an error that causes the program to fail spectacularly. See also logic error.

**logic chip** \loj'ik chip'\ *n.* An integrated circuit that processes information, as opposed to simply storing it. A logic chip is made up of logic circuits.

**logic circuit** \loj'ik sər'kət\ *n.* An electronic circuit that processes information by performing a logical operation on it. A logic circuit is a combination of logic gates. It produces output based on the rules of logic it is designed to follow for the electrical signals it receives as input. See also gate (definition 1).

**logic diagram** \loj'ik dī'ə-gram\ *n.* A schematic that shows the connections between computer logic circuits and specifies the expected outputs resulting from a specific set of inputs.

**logic error** \loj'ik ār'ər\ *n.* An error, such as a faulty algorithm, that causes a program to produce incorrect results but does not prevent the program from running. Consequently, a logic error is often very difficult to find. See also logic, semantics, syntax.

**logic gate** \loj'ik gāt\ *n.* See gate (definition 1).

**logic operation** \loj'ik op-ər-ā'shan\ *n.* An expression that uses logical values and operators; a bit-level manipulation of binary values. See also Boolean operator.

**logic programming** \loj'ik prō'gram-ēng\ *n.* A style of programming, best exemplified by Prolog, in which a program consists of facts and relationships from which the programming language is expected to draw conclusions. See also Prolog.

**logic-seeking printer** \loj'ik sē-kēng prin'tər\ *n.* Any printer with built-in intelligence that lets it look ahead of the current print position and move the print head directly to the next area to be printed, thus saving time in printing pages that are filled with spaces.

**logic symbol** \loj'ik sim'bəl\ *n.* A symbol that represents a logical operator such as AND or OR. For example, the symbol + in Boolean algebra represents logical OR, as in A + B (read, "A or B," not "A plus B").

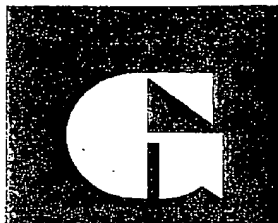
**logic tree** \loj'ik trē'\ *n.* A logic specification method that uses a branching representation. Each of the tree's forks represents a decision point; the ends of the branches denote actions to be taken.

**login** \log'in\ *n.* See logon.

**log in** \log in'\ *vb.* See log on.

**Logo** \lō'gō\ *n.* A programming language with features that are heavily drawn from LISP. Logo is often used to teach programming to children and was developed originally by Seymour Papert at

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**G** \gig'ə, jig'ə\ *prefix* See giga-

**.ga** \dot{G}-A'\ *n.* On the Internet, the major geographic domain specifying that an address is located in Gabon.

**GaAs** \G'A-A-S'\ *n.* See gallium arsenide.

**gain** \gān\ *n.* The increase in the amplitude of a signal, as of voltage, current, or power, that is produced by a circuit. Gain can be expressed as a factor or in decibels. *See also* decibel.

**gallium arsenide** \gal'ē-əm ār'sə-nīd\ *n.* A semiconductor compound used in place of silicon to make devices that perform faster, require less power, and are more tolerant of temperature changes and radiation than those made with silicon. *Also called* GaAs.

**game** \gām\ *n.* See computer game.

**game card** \gām' kārd\ *n.* See ROM card.

**game cartridge** \gām' kār'trij\ *n.* See ROM cartridge.

**Game Control Adapter** \gām' kən-trōl' ə-dap'tər\ *n.* In IBM personal computers and compatibles, a circuit that processes input signals at a game port. Devices such as joysticks and game paddles use potentiometers to represent their positions as varying voltage levels; the Game Control Adapter converts these levels to numbers using an analog-to-digital converter (ADC). *See also* analog-to-digital converter, game port, potentiometer.

**game port** \gām' pōrt\ *n.* In IBM personal computers and compatibles, an I/O port for devices such as joysticks and game paddles. The game port is often included with other I/O ports on a single expansion card. *See also* Game Control Adapter.

**game theory** \gām' thēr'ē, thē'ə-rē\ *n.* A mathematical theory, ascribed to John von Neumann, that considers strategy and probability in terms of competitive games in which all players have partial control and each seeks the most advantageous moves in relation to the others.

**Gantt chart** \gant' chārt\ *n.* A bar chart that shows individual parts of a project as bars against a horizontal time scale. Gantt charts are used as a project-planning tool for developing schedules. Most project-planning software can produce Gantt charts.

**gap** \gap\ *n.* *See* inter-record gap.

**garbage** \gär'baj\ *n.* Incorrect or corrupted data.

**garbage collection** \gär'baj kə-lek'shən\ *n.* A process for automatic recovery of heap memory. Blocks of memory that had been allocated but are no longer in use are freed, and blocks of memory still in use may be moved to consolidate the free memory into larger blocks. *See also* heap (definition 1).

**garbage in, garbage out** \gär'baj in' gär'baj out'\ *n.* A computing axiom meaning that if the data put into a process is incorrect, the data output by the process will also be incorrect. *Acronym:* GIGO (gī'gō, G'I-G-O').

**gas-discharge display** \gas'dis'chärj di-splā'\ *n.* A type of flat-panel display, used on some portable computers, containing neon between a horizontal and a vertical set of electrodes. When one electrode in each set is charged, the neon glows (as in a neon lamp) where the two electrodes intersect, representing a pixel. *Also called* gas-plasma display. *See also* flat-panel display, pixel.

**gas-plasma display** \gas'plā'zmə di-splā'\ *n.* *See* gas-discharge display.

**gate** \gāt\ *n.* 1. An electronic switch that is the elementary component of a digital circuit. It produces an electrical output signal that represents a binary 1 or 0 and is related to the states of one or more input signals by an operation of Boolean logic, such as AND, OR, or NOT. *Also called* logic gate. *See also* gate array. 2. The input terminal of a field-effect transistor (FET). *Also called* gate electrode. *See also* drain (definition 1), FET, MOSFET, source (definition 2). 3. A data structure used by 80386